WHAT IS CLAIMED IS:

1. A method of forming a nonvolatile memory device, the method comprising:

forming a tunnel insulation pattern and a first floating gate pattern that are sequentially stacked on a semiconductor substrate;

forming a trench in the semiconductor substrate;

forming a device isolation layer in the trench;

sequentially forming an etch stop layer and a mold layer on the device isolation layer and on the first floating gate pattern; and

successively patterning the mold layer and the etch stop layer to form a groove exposing at least the first floating gate.

2. The method of claim 1, further comprising:

forming a second floating gate pattern that fills the groove.

3. The method of claim 1, wherein forming the first floating gate pattern and the trench comprises:

sequentially forming a tunnel insulation layer, a first floating gate conductive layer, and a hard mask layer on the semiconductor substrate;

successively patterning the hard mask layer, the first floating gate conductive layer, and the tunnel insulation layer to expose a region of the semiconductor substrate, thereby forming a tunnel insulation pattern, a first floating gate pattern, and a hard mask pattern; and

selectively etching the exposed region of the semiconductor substrate to form the trench therein.

4. The method of claim 3, wherein forming the device isolation layer comprises:

forming a device isolation insulating layer that fills the trench;

planarizing the device isolation insulating layer, until the hard mask pattern is exposed, thereby forming a device isolation layer in the trench; and

etching the exposed hard mask layer until the first floating gate pattern is exposed.

5. The method of claim 1, wherein the etch stop layer is formed of a material having an etch selectivity with respect to the device isolation layer and the first floating gate pattern.

6. The method of claim 5, wherein the etch stop layer is formed of silicon nitride.

7. The method of claim 1, wherein the mold layer is formed of a material having an etch selectivity with respect to the etch stop layer.

8. The method of claim 7, wherein the mold layer is formed of silicon oxide.

9. The method of claim 1, wherein forming the groove comprises:

forming a photoresist pattern on the mold layer, wherein the photoresist pattern comprises an opening that exposes a region of the mold layer;

isotropically etching the mold layer to form a preliminary groove that exposes the etch stop layer overlying the first floating gate pattern, using the photoresist pattern as a mask;

removing the photoresist pattern from the semiconductor substrate; and

etching the etch stop layer exposed in the preliminary groove to form the groove exposing at least the first floating gate pattern.

10. The method of claim 9, wherein the groove is wider than the opening.

11. The method of claim 2, wherein forming the second floating gate pattern comprises:

forming a second floating gate conductive layer on the semiconductor substrate to fill in the groove; and

planarizing the second floating gate conductive layer to expose the patterned mold layer, thereby forming the second floating gate pattern within the groove.

12. The method of claim 1, wherein the first and second floating gate patterns are formed of doped polysilicon.

13. The method of claim 11, further comprising:

etching the patterned mold layer and the patterned etch stop layer until the device isolation layer is exposed;

conformally forming a control gate insulation layer and a control gate conductive layer on the semiconductor substrate including the second floating gate pattern; and

successively patterning the control gate conductive layer, the control gate insulation layer, the second floating gate pattern, and the first floating gate pattern to form first and second floating gate electrodes, a control gate insulation pattern, and a control gate that are sequentially stacked, wherein the first and second floating gate electrodes form a floating gate.

14. A method of forming a nonvolatile memory device, the method comprising:

forming a tunnel insulation pattern and a first floating gate pattern that are sequentially stacked on a semiconductor substrate;

forming a trench in the semiconductor substrate;

forming a device isolation layer in the trench;

sequentially forming an etch stop layer and a mold layer on the device isolation layer and on the first floating gate pattern;

successively patterning the mold layer and the etch stop layer to form a groove exposing at least the first floating gate;

forming a second floating gate conductive layer on the semiconductor substrate to fill in the groove;

planarizing the second floating gate conductive layer to expose the patterned mold layer, thereby forming a second floating gate pattern within the groove;

removing the patterned mold layer and the patterned etch stop layer until the device isolation layer is exposed;

conformally forming a control gate insulation layer and a control gate conductive layer overlying the second floating gate pattern; and

successively patterning the control gate conductive layer, the control gate insulation layer, the second floating gate pattern, and the first floating gate pattern to form a floating gate, a control gate insulation pattern, and a control gate.